**Design Simulation Activity**

1. **Simulated results -> input V vs Output V**

A screen shot of a computer

AI-generated content may be incorrect.

**Draw Backs**

* Resistor RS gives a negative feedback to the input side. It will reduces the voltage VGS . Therefore Voltage gain will be reduced
* The Q point is not at the middle of the DC load line. If the input voltage amplitude is increased the output voltage will clipped off

**A screen shot of a computer

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Out put negative half cycle clipped off

1. **design improvents**

in the j fet the idss = 9.116 mA so to set Q point in the middel of the DC load line chosen the Id as idss/2=4.558 mA . then calculated VGS = - 0.5858V . from that we got Rs = 0.1285k , Rd = 0.8588k . this improvements moved Q point to the middle of Dc load line. modify this text